CLAIMS

Please amend the claims as follows:

1. (currently amended) A system for processing applications, the system comprising:

a plurality of processor nodes with each processor node comprising[[:]]

a processing element configured to execute at least one of the applications,

a software extensible device configured to provide additional previously presented instructions to a set of standard instructions for the processing element, wherein the previously presented instructions can be programmed by software,

a first communication interface including

a first selector module configured to communicate with a first other member of the plurality of processor nodes or communicate with a first input/output device,

a first array interface module configured to ~~interface to a~~ communicate with the first other member of the plurality of processor nodes via the first selector module,

a first standard input/output interface configured to communicate with ~~a~~ the first input/output device via the first selector module, the first selector module further configured to select between the first array interface module and the first standard input/output interface,

a second communication interface including

a second selector module configured to communicate with a second other member of the plurality of processor nodes or communicate with a second input/output device,

a second array interface module configured to ~~interface to a~~ communicate with the second other member of the plurality of processor nodes via the second selector module,

a second standard input/output interface configured to communicate with ~~a~~ the second input/output device via the second selector module, the second selector module further configured to select between the second array interface module and the second standard input/output interface; and

a plurality of links interconnecting the plurality of processor nodes.

2. (previously presented) The system of claim 1 wherein each one of the processor nodes are on separate chips.

3. (previously presented) The system of claim 1 wherein at least two of the processor nodes are on the same chip.

4. (previously presented) The system of claim 1 wherein two or more of the plurality of the processor nodes are configured in an array.

5. (original) The system of claim 1 wherein the software extensible device comprises an instruction set extension fabric.

6. (original) The system of claim 1 wherein the software extensible device comprises a programmable logic device.

7. (canceled)

8. (previously presented) The system of claim 1 wherein at least one of the first communication interface and the second communication interface is configured to communicate using message passing.

9. (previously presented) The system of claim 1 wherein at least one of the first communication interface and the second communication interface is configured to communicate using channels between the processor nodes.

10. (previously presented) The system of claim 9 wherein at least one of the first communication interface and the second communication interface is configured to perform time division multiplexing using the channels between the processor nodes.

11. (previously presented) The system of claim 9 wherein at least one of the first communication interface and the second communication interface is configured to perform spatial division multiplexing using the channels between the processor nodes.

12. (previously presented) The system of claim 1 wherein at least one of the first communication interface and the second communication interface comprises a processor network interface.

13. (previously presented) The system of claim 1 wherein at least one of the first communication interface and the second communication interface comprises a processor network switch.

14. (previously presented) The system of claim 1 wherein at least one of the first communication interface and the second communication interface comprises a standard input/output interface configured to receive the additional previously presented instructions.

15. (canceled)

16. (currently amended) The system of claim 1 wherein at least one of the first ~~communication interface~~selector module and the second ~~communication interface~~selector module comprises a multiplexer/demultiplexer.

17. (canceled)

18. (currently amended) A method for a system with multiple processor nodes, the method comprising:

executing an application in at least one processing element in a plurality of the processor nodes;

providing an additional previously presented instruction to a set of standard instructions for the processing element, using at least one software extensible device in the plurality of the processor nodes, wherein the previously presented instructions can be programmed by software;

communicating using a ~~first~~ communication interface including a ~~first array interface~~selector module configured to ~~interface~~ communicate to a neighboring device that is a~~first other~~ member of the plurality of processor nodes or a neighboring device that is not a member of the plurality of processor nodes, the selector module further configured to select between an array interface module and a standard input/output interface;

determining if ~~a~~ the neighboring device is a member of the plurality of processor nodes or is a not a member of the plurality of processor nodes;

if the neighboring device is a member of the plurality of processor nodes, selecting the array interface module for communicating to the neighboring device via the selector module ~~using a second communication interface including a second array interface module~~; and

if the neighboring device is not a member of the plurality of processor nodes, selecting the standard input/output interface for

communicating to the neighboring device via the selector module ~~using a standard input/output interface of the second communication interface~~.

19. (canceled)

20. (currently amended) The method of claim 18 wherein communicating using a ~~first~~ communication interface ~~including a first array interface module~~ comprises using message passing.

21. (currently amended) The method of claim 18 wherein communicating using a ~~first~~ communication interface ~~including a first array interface module~~ comprises using channels between the processor nodes.

22. (original) The method of claim 21 wherein using the channels between the processor nodes further comprises performing time division multiplexing with the channels.

23. (original) The method of claim 21 wherein using the channels between the processor nodes further comprises performing spatial division multiplexing with the channels.

24. (original) The method of claim 18 further comprising compiling the application.

25. (original) The method of claim 18 further comprising loading the application into one of the plurality of the processor nodes.

26. (currently amended) The method of claim 18 ~~further comprising configuring one of the processor nodes to select between an array interface module and a~~ wherein selecting the standard input/output interface for

communicating to the neighboring device via the selector module comprises configuring the selector module to select the standard input/output interface for communicating to the neighboring device via the selector module ~~based on a type of the neighboring device~~.

27-30. (canceled)

31. (currently amended) The system of claim 1 wherein each processor node further comprises:

a third communication interface including

a third selector module configured to communicate with a third other member of the plurality of processor nodes or communicate with a third input/output device,

a third array interface module configured to ~~interface to~~ communicate with a third other member of the plurality of processor nodes via the third selector module, and

a third standard input/output interface configured to communicate with a third input/output device via the third selector module, the third selector module further configured to select between the third array interface module and the third standard input/output interface, and

a fourth communication interface including

a fourth selector module configured to communicate with a fourth other member of the plurality of processor nodes or communicate with a fourth input/output device,

a fourth array interface module configured to ~~interface to~~communicate with a fourth other member of the plurality of processor nodes via the fourth selector module, and

a fourth standard input/output interface configured to communicate with a fourth input/output device via the fourth selector module, the fourth selector module further configured to select between the fourth array interface module and the fourth standard input/output interface.

32. (previously presented) The system of claim 1 wherein the first communication interface is configured to communicate through the first array interface module if the first communication interface is coupled to the first other member of the plurality of processor nodes, and to communicate through the first standard input/output interface if the first communication interface is coupled to the first input/output device.

33. (previously presented) The system of claim 1 wherein two or more of the plurality of processor nodes are configured in a one-dimensional array.

34. (previously presented) The system of claim 1 wherein three or more of the plurality of the processor nodes are configured in a non-rectangular configuration.

35. (previously presented) The system of claim 10 wherein the time division multiplexing provides a guaranteed bandwidth for a communication between the processor nodes.

36. (previously presented) The system of claim 1 wherein the first communication interface is configured to guarantee a bandwidth for a communication between two of the plurality of processor nodes.

37. (currently amended) The method of claim 18 further comprising:

determining if another neighboring device is a member of the plurality of processor nodes;

if the another neighboring device is a member of the plurality of processor nodes, selecting a second array interface module for communicating to the another neighboring device via a second selector module ~~using a third communication interface including a third array interface module~~; and

if the another neighboring device is not a member of the plurality of processing nodes, selecting a second standard input/output interface for communicating to the neighboring device via the second selector module ~~using a standard input/output interface of the third communication interface~~.

38. (currently amended) The method of claim 18 wherein the communicating using the ~~first~~ communication interface uses the ~~first~~ array interface module and uses time division multiplexing, the time division multiplexing providing a guaranteed bandwidth for a communication to the ~~first~~ other member of the plurality of processor nodes.

39. (new) The method of claim 18 wherein selecting the array interface module for communicating to the neighboring device via the selector module comprises configuring the selector module to select the standard input/output interface for communicating to the neighboring device via the selector module.

40. (new) The system of claim 18 wherein the selector module comprises a multiplexer/demultiplexer.